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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/759,270	01/20/2004	Ho-Rang Jang	2557-000204/US	6847

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EXAMINER

YU, JAE UN

ART UNIT	PAPER NUMBER
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2185

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/25/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary

Application No.

10/759,270

Applicant(s)

JANG, HO-RANG

Examiner

Jae U. Yu

Art Unit

2185

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 30 October 2006.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-26 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-4, 10, 11, 13, 17-19, 22, 23, 25 and 26 is/are rejected.
- 7) ☒ Claim(s) 5-9, 12-16, 20-21 and 24 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETEAILED ACTION

The examiner acknowledges the applicant's submission of the amendment dated 10/30/2006. At this point claims 1-26 are pending in the instant application.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

1. Claims 1-4, 17-19, 22, 23 and 26 are rejected under 35 USC 103 (a) as being obvious over Morikawa et al. (US 2001/0032297) in view of Rosner et al. (US 2004/0221138).
2. As per independent claim 1, Morikawa et al. disclose, "a first cache memory [**"L2 Cache" 9, Figure 1**] for enabling a running flag signal [**Setting the "target flag" to "0", Paragraph 35**] in response to a given interrupt signal from a DSP core of the DSP [**"Prefetch Instruction" 31 from the "Processor" 1, Figure 2**] to provide a given number of first instructions to the DSP core [**Providing data to the "naked cache" 34, Figure 3**], and for disabling the running flag signal [**Setting the "target flag" to "1", Paragraph 38**]", and "a second cache memory" [**"Cache-miss Cache" 7, Figure 2**] for providing second instruction to the processor [**Paragraph 38**] when the "running flag signal is disabled [**Setting the "target flag" to "1", Paragraph 38**]".

Morikawa et al. do not disclose expressly that the data being transferred from/to are "instructions".

Rosner et al. disclose, "loading instructions fetched from memory into an instruction cache for faster subsequent retrieval" in paragraph 26.

Morikawa et al. and Rosner are analogous art because they are from the same filed of endeavor of data processing.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify Morikawa et al. by including an "instruction cache" as taught by Rosner et al. in paragraph 26.

The motivation for doing so would have been "increased efficiency" and "faster instruction retrieval" as expressly taught by Rosner et al. in paragraph 26.

Therefore, it would have been obvious to combine Rosner et al. with Morikawa et al. for the benefit of efficient and fast instruction retrieval to obtain the invention as specified in claim 1.

3. As per **independent claim 17**, Morikawa et al. disclose, "a first cache memory [**"Naked Cache" 6, Figure 1**] providing a first instruction in response to a program address [**"Prefetch Instruction" 31, Figure 3**] received from a DSP core of the DSP

["Processor" 1, Figure 1], if there is no first instruction corresponding to the program address, and outputting a first miss signal **["Cache Miss" 32, Figure 3]**.

"A second cache memory **["Cache-miss cache" 7, Figure 1]** providing at least one second instruction to the DSP core **[Providing data to the "processor" 37, Figure 3]** in response to a given interrupt signal **[Step 31, Figure 3]** and the first miss signal **["Cache Miss" 35, Figure 3]** and, the second cache memory further disabling a running flag signal based after a given number of second instructions have been provided to the DSP core" **Setting the "target flag" to "1" (Paragraph 38)** corresponds to "enabling a running flag signal", which enables the "Cache-miss cache" ("Second cache memory"). Therefore, setting the "target flag" to "0" (Paragraph 35) corresponds to "disabling a running flag signal", which disables the "Cache-miss cache" ("Second cache memory") and enables the "naked cache".

"A third cache memory **["L2 Cache" 9, Figure 1]** which provides a third instruction to the DSP core **[Prefetching data to the "naked cache" (Step 34, Figure 3), which will be provided to the "processor" (Figure 1)]** in response to the first miss signal **["Cache Miss" 32, Figure 3]**, when the running flag signal is disabled **[Setting the "target flag" to "0", Paragraph 35]**"

Morikawa et al. do not disclose expressly that the data being transferred from/to are "instructions".

Rosner et al. disclose, "loading instructions fetched from memory into an instruction cache for faster subsequent retrieval" in paragraph 26.

Morikawa et al. and Rosner are analogous art because they are from the same filed of endeavor of data processing.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify Morikawa et al. by including an "instruction cache" as taught by Rosner et al. in paragraph 26.

The motivation for doing so would have been "increased efficiency" and "faster instruction retrieval" as expressly taught by Rosner et al. in paragraph 26.

Therefore, it would have been obvious to combine Rosner et al. with Morikawa et al. for the benefit of efficient and fast instruction retrieval to obtain the invention as specified in claim 17.

4. **Claims 2 and 18** disclose, "a first interface [**"Data Block Buffer" 18, "Multiplexer" 16 and "Address Buffer" 13, Figure 2]** unit which interfaces the DSP core [**"Processor", Figure 2]**, first cache memory [**"Naked Cache", Figure 2]**, second cache memory [**"Cache-miss Cache", Figure 2]** and third cache memory [**"L2 Cache", Figure 2]**".

"A second interface unit [**"Target Flag" 19, "Target Switch" 20 and "Multiplexer" 16, Figure 2]** which interfaces the first cache memory, second cache memory, third cache memory and a program memory [**"Register File", Figure 1]** that stores instructions for the DSP core"

5. **Claim 3** discloses, "the given number of first instructions enable the DSP core to check a state of the interrupt request [**"Prefetch Instruction?" 31, Figure 3, Morikawa et al.]** and to read relevant input variables [**Read from cache (Step 32, 35, Figure 3), Morikawa et al.]**".

6. **Claims 4 and 19** disclose, "a cache memory block [**"Data", Figure 2, Morikawa et al.]** which stores a given one of the given number of first instructions received from the program memory [**Prefetching, Figure 3, Morikawa et al.]** in response to a corresponding write address and outputs each one of the given number of first instructions [**Step 36, Figure 3, Morikawa et al.]** in response to a corresponding read address".

"A cache controller which generates the write address [**Step 37, Figure 3]**, read address [**Step 36, Figure 3, Morikawa et al.]**, and a prefetch address [**Prefetching, Figure 3, Morikawa et al.]** using a program address received from the DSP core via the first interface unit, wherein the cache controller transmits the prefetch address to the

program memory via the second interface unit in order to receive a given first instruction
[Step 34, Figure 3]"

7. As per independent claim 22, Morikawa et al. disclose, "(a) first providing a first instruction from a first cache memory **[Providing data from "Naked Cache" 6, Figure 1]** to a DSP core **["Processor" 1, Figure 1]** in response to a program address received from the DSP core **["Prefetch Instruction" 31, Figure 3]"**.

"(b) second providing at least one second instruction from a second cache memory **["Cache-miss cache" 7, Figure 1]** to the DSP core **[Providing data to the "processor" 37, Figure 3]** in response to the program address based on at least one of an output of a first miss signal **["Cache Miss" 35, Figure 3]** from the first cache memory and an enabling of a running flag signal by the second cache memory" **Setting the "target flag" to "1" (Paragraph 38) corresponds to "enabling a running flag signal", which enables the "Cache-miss cache" ("Second cache memory")**.

"(c) disabling the running flag signal and ceasing step (b) when a number of second instructions provided to the DSP core reaches a given value **[Single data transfer (Figure 3)]**" **Setting the "target flag" to "1" (Paragraph 38) corresponds to "enabling a running flag signal", which enables the "Cache-miss cache" ("Second cache memory")**. Therefore, setting the "target flag" to "0" (Paragraph

35) corresponds to “disabling a running flag signal”, which disables the “Cache-miss cache” (“Second cache memory”) and enables the “naked cache”.

“(d) third providing a third instruction from a third cache memory [“L2 Cache” 9, Figure 1] to the DSP core [Prefetching data to the “naked cache” (Step 34, Figure 3), which will be provided to the “processor” (Figure 1)] in response to the program address based on at least one the first miss signal output [“Cache Miss” 32, Figure 3] from the first cache memory and a disabling of the running flag signal [Setting the “target flag” to “0”, Paragraph 35] by the second cache memory”

“(e) enabling the running flag signal at the second cache memory when an interrupt signal is received thereto from the DSP core [Step 31, Figure 3]” Setting the “target flag” to “1” (Paragraph 38) corresponds to “enabling a running flag signal”, which enables the “Cache-miss cache” (“Second cache memory”).

8. **Claim 23 disclose, “repeating” claims 10 and 22 “iteratively until there are no further instruction requests from the DSP core”. Morikawa et al. performs the steps in Figure 3 for each instruction requests from the processor.**

9. **Claim 26 disclose, “a cache memory device for a digital signal processor that is controlled in accordance with the method of claim 22 [Figures 1-3, Morikawa et al.]”.**

10. Claims 10, 11, 13 and 25 are rejected under 35 USC 103 (a) as being obvious over Morikawa et al. (US 2001/0032297) in view of Rosner et al. (US 2004/0221138) and Chiu et al. (US 6,505,253).

11. As per **independent claim 10**, Morikawa et al. disclose, "(a) first providing an instruction to a DSP core of the DSP from a cache memory [**Providing data to the "naked cache" from "L2 Cache" (Element 9, Figure 1) 34, Figure 3**], in response to a request from the DSP core [**"Prefetch Instruction" 31 from the "Processor" 1, Figure 2**].

"(b) enabling a running flag signal [**Setting the "target flag" to "1", Paragraph 38**] in another cache memory [**"Cache-miss Cache" 7, Figure 1**] in response to an interrupt signal [**"Load Instruction" from the "processor", Paragraph 38**] received thereto from the DSP core"

"(c) second providing, in response to a request from the DSP core [**"Load Instruction" from the "processor", Paragraph 38**], a given number of instructions from the another cache memory to the DSP core [**Providing data from the "cache-miss cache" to the "processor" 37, Figure 3**] that are different from the first provided instruction [**Since the data transfer (Step 37, Figure 3) is caused by the cache miss in step 35, the data in step 37 is different from the prefetched data in step 34**]"

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“(d) disabling the running flag signal [Setting the “target flag” to “0”, Paragraph 35]”

Morikawa et al. do not disclose expressly that the data being transferred from/to are “instructions”.

Rosner et al. disclose, “loading instructions fetched from memory into an instruction cache for faster subsequent retrieval” in paragraph 26.

Morikawa et al. and Rosner et al. do not disclose expressly, “ceasing said second providing step when the given number of instructions reaches a threshold value”.

Chiu et al. disclose stop sending new data to a cache (“second providing step”) when the cache fills up above a threshold value in column 19, at lines 40-43.

Morikawa et al., Rosner and Chiu et al. are analogous art because they are from the same filed of endeavor of data processing.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify Morikawa et al. by including an “instruction cache” as taught by Rosner et al. in paragraph 26 and stop sending new data to a cache when the cache fills up above a threshold value as taught by Chiu et al. in column 19, at lines 40-43.

The motivation for doing so would have been “increased efficiency”, “faster instruction retrieval” as expressly taught by Rosner et al. in paragraph 26 and to “free some buffers from the cache” as expressly taught by Chiu et al. in column 19, at lines 40-43.

Therefore, it would have been obvious to combine Rosner et al. and Chiu et al. with Morikawa et al. for the benefit of efficient, fast instruction retrieval and freeing buffers from a cache to obtain the invention as specified in claim 2.

12. **Claim 11** discloses, “repeating” claim 10 “iteratively until there are no further instruction requests from the DSP core”. **Morikawa et al. performs the steps in Figure 3 for each instruction requests from the processor.**

13. **Claim 13** discloses, “(f) determining whether or not the given number of instructions in step (c) reaches the given value based on the accumulated count value”. **Chiu et al. disclose stop sending new data to a cache (“second providing step”) when the cache fills up above a threshold value in column 19, at lines 40-43.**

14. **Claim 25** discloses, “a cache memory device for digital signal processor that is controlled in accordance with the method of claim 10 [Figure 1-3, Morikawa et al.]”.

Arguments Concerning Prior Art Rejections

1st Point of Argument

Regarding independent claim 1, the applicant argues that Morikawa fails to teach the “first cache memory” enabling the target flag. However, the examiner considers the “target flag” (Paragraph 35) as a part of the “first cache memory”. Since the “target flag” is enabled within the “first cache memory”, Morikawa clearly anticipates the claim limitation.

2nd Point of Argument

Regarding independent claim 2, the applicant further argues that Morikawa’s “Processor 1” and “naked cache” do not correspond to the “digital signal processor (DSP)”, because the “naked cache” is simply a data storage device. However, the examiner interprets the “DSP” as any apparatus that is capable of processing digital signals (i.e. a computer). Moreover, a computer processor embodying a data storage device (i.e. registers) is extremely well known in the art. Therefore, the naked cache being “simply a data storage device” is not a persuasive argument because the examiner considers it as a part of a processing core (Processor 1 and naked cache).

3rd Point of Argument

Regarding independent claim 17, the applicant argues that Morikawa does not teach an instruction cache (Page 11, Remarks). However, the examiner directs the

applicant's attention to corresponding claim rejection above. The claim rejection clearly indicates an **instruction cache disclosed in Rosner et al.**

4th Point of Argument

Regarding claim 10, the applicant argues that the "Load Instruction" is not equivalent to "an interrupt signal". However, the examiner considers an "interrupt signal" is broader in scope than the "Load Instruction" (Paragraph 38, Morikawa et al.). (i.e. An "interrupt signal" is any form of signal that "interrupts" a system to perform certain tasks.)

Further, the "Load Instruction" triggers the "Cache Hit?" determination step (Element 35, Figure 3), wherein the naked cache miss ("No", Step 35) corresponds to the data transfer "request from the DSP core".

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

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the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

A. Status of Claims in the Application

The following is a summary of the treatment and status of all claims in the application as recommended by M.P.E.P. 707.07(i).

Allowable Subject Matter

1. Claims 5-9, 12-16, 20-21 and 24 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.
2. The primary reasons for allowance of claims 5-9, 12-16, 20-21 and 24 in the instant application is the combination with the inclusion in these claims that "the cache controller" and its corresponding method (Claims 5 and 12) and "the cache controller" and its corresponding method (Claims 20 and 24). The prior art of record neither anticipates nor renders obvious the above recited combination.
3. As allowable subject matter has been indicated, applicant's response must either comply with all formal requirements or specifically traverse each requirement not complied with. See 37 C.F.R. § 1.111(b) and § 707.07(a) of the M.P.E.P.

Claims Rejected in the Application

Per the instant office action, claims 1-4, 10, 11, 13, 17-19, 22, 23, 25 and 26 have received a second action on the merits and are subject of a second action final.

B. Directions of Future Correspondences

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jae Un Yu who is normally available from 9:00 A.M. to 5:30 P.M. Monday thru Friday and can be reached at the following telephone number: (571) 272-1133.


If attempts to reach the above noted examiner by telephone are unsuccessful, the Examiner's supervisor, Sanjiv Shah, can be reached at the following telephone number: (571) 272-4098.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

January 11, 2007

Jae Un Yu

Art Unit 2185


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